AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Currently Amended) ~~The apparatus of claim 1~~ An apparatus for controlling the decision threshold level of a decision circuit in a burst-mode receiver, comprising:

an averaging filter circuit configured to receive a burst-mode data transmission signal, said averaging filter circuit operable to output an average value of said burst-mode data transmission signal; and

a control circuit coupled to said averaging filter circuit, said control circuit operable to couple said average value of said burst-mode data transmission signal acquired during a preamble portion of said burst-mode data transmission signal to said decision threshold level during substantially all of a payload portion of said burst-mode data transmission signal, wherein said control circuit comprises a track and hold circuit operable in response to a switchable track enable signal to track said average threshold value of said burst-mode data transmission signal during said preamble portion of said burst-mode data transmission signal and otherwise to hold said average threshold value of said average value of said burst-mode data transmission signal acquired during said preamble portion of said input signal and to couple said held average threshold value to said decision threshold voltage level during substantially all of said payload portion.

3. (Previously Presented) An apparatus for controlling the decision threshold level of a decision circuit in a burst-mode receiver, comprising:

an averaging filter circuit configured to receive a burst-mode data transmission signal, said averaging filter circuit operable to output an average value of said burst-mode data transmission signal; and

a control circuit coupled to said averaging filter circuit, said control circuit operable to couple said average value of said burst-mode data transmission signal acquired during a preamble portion of said burst-mode data transmission signal to said decision threshold level during substantially all of a payload portion of said burst-mode data transmission signal, wherein said control circuit comprises a track and hold circuit operable in response to a switchable track enable signal to track said average threshold value of said burst-mode data transmission signal during said preamble portion of said burst-mode data transmission signal and otherwise to hold said average threshold value of said average value of said burst-mode data transmission signal acquired during said preamble portion of said input signal and to couple said held average threshold value to said decision threshold voltage level during substantially all of said payload portion, and wherein said control circuit further comprises a phase-locked loop circuit coupled with said track and hold circuit, said phase-locked loop circuit operable to repetitively switch said track enable signal in response to a repetitive dark time synchronization input pulse.

4. (Original) The apparatus of claim 3 wherein said phase-locked loop circuit comprises circuitry selected from the group consisting of all-digital circuitry, analog circuitry, and hybrid digital and analog circuitry.

5. (Original) The apparatus of claim 3 wherein said repetitively switched track enable signal occurs before said repetitive dark time synchronization input pulse relative to said preamble portion of said data signal.

6. (Original) The apparatus of claim 3 operable to receive a data signal having a data transmission rate of approximately 12.5 gigabit per second .

7. (Original) The apparatus of claim 3 wherein said control circuit further comprises a dark time detector circuit coupled with said phase-locked loop circuit, said dark time detector circuit operable to generate said repetitive dark time synchronization pulse at regular intervals in response to the instantaneous amplitude of said data signal relative to a peak amplitude of said data signal during a dark period prior to said preamble portion.

8. (Original) The apparatus of claim 7 wherein said dark time detector circuit comprises a precision peak detector circuit coupled with said photodetector circuit, said precision peak detector circuit operable to detect said peak amplitude of said data signal during said dark period and to output a DC voltage signal proportional to said peak amplitude.

9. (Original) The apparatus of claim 8 wherein said dark time detector circuit further comprises a comparator circuit coupled with said precision peak detector circuit, said averaging filter circuit, and said phase-locked loop circuit, said comparator circuit operable to intercompare respective input voltages from said precision peak detector circuit and said averaging filter circuit and in response thereto to output said repetitive dark time synchronization pulse.

10. (Canceled)

11. (Original) A method of processing in a receiver a burst-mode input signal having a preamble portion and a payload portion, said method comprising the steps of:

converting said input signal into a first voltage signal;

converting said first voltage into a second voltage signal in response to a decision threshold voltage level;

averaging said first voltage signal using an averaging frequency lower than the transmission bit rate of said input signal and higher than the burst frequency of said burst-mode input signal, to convert said first voltage signal into an average threshold value of said first voltage signal; and

coupling said average threshold value of said first voltage converted during said preamble portion to said decision threshold voltage level during substantially all of said payload portion of said input signal.

12. (Original) The method of claim 11 wherein said transmission bit rate is approximately 12.5 gigabits per second.

13. (Original) The method of claim 11 wherein said coupling of said average threshold value occurs in response to a repetitive signal switched synchronously with said burst frequency of said burst-mode input signal.

14. (Original) The method of claim 13 wherein said synchronously switched repetitive signal is generated in a phase-locked loop circuit in response to a repetitive synchronization input pulse.

15. (Original) The method of claim 14 wherein said phase-locked loop circuit comprises circuitry selected from the group consisting of all-digital circuitry, analog circuitry, and hybrid digital and analog circuitry.

16. (Original) The method of claim 14 wherein said synchronously switched repetitive signal occurs prior to said repetitive synchronization input pulse relative to said preamble portion of said input signal.

17. (Original) The method of claim 11 wherein said receiver is an optical receiver.

18. (Original) A communication system configured for processing a burst-mode input signal having a preamble portion and a payload portion, said system incorporating:

a burst-mode receiver comprising:

a photodetector circuit operable to convert a burst-mode input signal into a first voltage signal, said input signal having a preamble portion and a payload portion;

a limiting amplifier circuit interconnected with said photodetector circuit and having a control port, said limiting amplifier circuit operable to convert said first voltage signal into a second voltage signal in response to a decision threshold voltage level at said control port;

an averaging filter circuit interconnected with said photodetector circuit, said averaging filter circuit operable to convert said first voltage signal into an average value of said first voltage signal; and

a control circuit interconnected with said averaging filter circuit, said control circuit operable to couple said average value of said first voltage converted during said preamble portion of said input signal to said decision threshold voltage level at said control port during substantially all of said payload portion of said input signal.

19. (Original) The system of claim 18 wherein said control circuit comprises a track and hold circuit operable in response to a switchable track enable signal to track said average value of said first voltage during said preamble portion of said input signal and otherwise to hold said average value of said first voltage converted during said preamble portion of said burst-mode signal and to couple said held average value to said decision threshold voltage level at said control port.

20. (Previously Presented) A communication system configured for processing a burst-mode input signal having a preamble portion and a payload portion, said system incorporating:

a burst-mode receiver comprising:

a photodetector circuit operable to convert a burst-mode input signal into a first voltage signal, said input signal having a preamble portion and a payload portion;

a limiting amplifier circuit interconnected with said photodetector circuit and having a control port, said limiting amplifier circuit operable to convert said first voltage signal into a second voltage signal in response to a decision threshold voltage level at said control port;

an averaging filter circuit interconnected with said photodetector circuit, said averaging filter circuit operable to convert said first voltage signal into an average value of said first voltage signal; and

a control circuit interconnected with said averaging filter circuit, said control circuit operable to couple said average value of said first voltage converted during said preamble portion of said input signal to said decision threshold voltage level at said control port during substantially all of said payload portion of said input signal, wherein said control circuit comprises a track and hold circuit operable in response to a switchable track enable signal to track said average value of said first voltage during said preamble portion of said input signal and otherwise to hold said average value of said first voltage converted during said preamble portion of said burst-mode signal and to couple said held average value to said decision threshold voltage level at said control port, and wherein said control circuit further comprises a phase-locked loop circuit interconnected with said track and hold circuit, said phase-locked loop circuit operable to repetitively switch said track enable signal in response to a repetitive dark time synchronization input pulse.

21. (Original) The system of claim 20 wherein said phase-locked loop circuit comprises circuitry selected from the group consisting of all-digital circuitry, analog circuitry, and hybrid digital and analog circuitry.

22. (Original) The system of claim 20 wherein said repetitively switched track enable signal occurs before said repetitive dark time synchronization input pulse relative to said preamble portion of said input signal.

23. (Original) The system of claim 18 operable to receive an input signal having a data transmission rate of approximately 12.5 gigabit per second.

24. (Original) The system of claim 20 wherein said control circuit further comprises a dark time detector circuit interconnected with said phase-locked loop circuit, said dark time detector circuit operable to generate said repetitive dark time synchronization pulse at regular intervals in response to the instantaneous amplitude of said burst-mode signal relative to a peak amplitude of said burst-mode signal during a dark period prior to said preamble portion.

25. (Previously Presented) The system of claim 24 wherein said dark time detector circuit comprises a precision peak detector circuit interconnected with said photodetector circuit, said precision peak detector circuit operable to detect said peak amplitude of said burst-mode signal during said dark period and to output a DC voltage signal proportional to said peak amplitude.

26. (Original) The system of claim 25 wherein said dark time detector circuit further comprises a comparator circuit interconnected with said precision peak detector circuit, said averaging filter circuit, and said phase-locked loop circuit, said comparator circuit operable to intercompare respective input voltages from said precision peak detector circuit and said averaging filter circuit and in response thereto to output said repetitive dark time synchronization pulse.

27. (Original) The system of claim 18 further comprising a router apparatus.

28. (Original) The system of claim 18 wherein said system is an optical communication system.